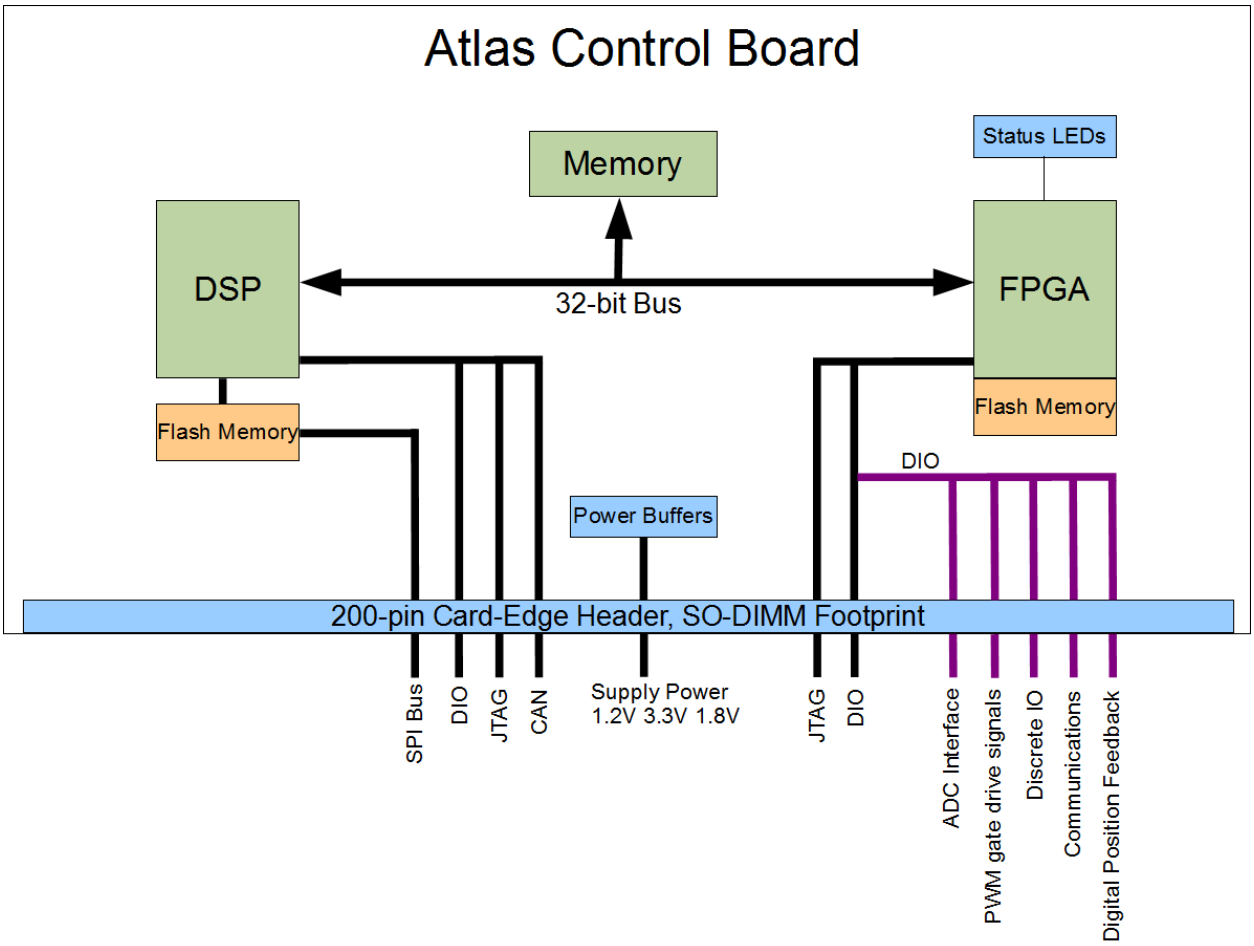
3L Power Atlas Control Board in Motor Control Configuration

Block Diagram of 3L Atlas Control Board



Functional and Performance

PWM

The PWM state machine exists in FPGA firmware, and can be configured for frequencies between 0 Hz and 1 MHz, with variable deadtimes. 3-phase, 2-level, and 3-level state machines are available.

Current/Torque Control

Typical motor control configurations include an inner torque / current control algorithm that relies on a current command, 3-phase feedback current, and a PI regulator that tries to match the actual current to the current command. Depending on the amount of other tasks running, the control loop can run between 10 Hz up to 50 kHz. Control loop gains are not limited, and can be set by parameter adjustment. Current PI regulator gains Kp and Ki have units of Volts/Amp and Volts/Amp-second respectively, and the resulting system bandwidth is dependent on other parameters, such as input voltage and output (load) impedance.

Current feedback sampling rates are highly dependent on hardware, and should at least be as fast as the desired torque control loop frequency. If separate hardware-based overcurrent fault detection is not included, then the sampling rate should be at least 200 kHz to allow for adequate firmware-based fault detection. Sampling rates up to 1 MHz per channel are possible with appropriate ADC hardware.

Raw current feedback signals can be filtered with user-settable bandwidth, processed through a real-time RMS calculation, and processed through a DQ0 transform.

Velocity Control

Typical motor control configurations include an outer velocity control algorithm that relies on a velocity command, position feedback, and a PI regulator that tries to match the actual position time-derivative to the velocity command. The output of the PI regulator is a current command that is fed into the torque / current regulator, and this output has both negative and positive limits that are user-settable. As with the current regulator, the control loop can update at rates between 10 Hz and 50 kHz. Although PI regulator gains, Kp and Ki, are settable per user requirements, the regulator can go unstable if the velocity control regulator is faster than the inner loop current regulator.

Position feedback is fed to the Atlas board FPGA pins, and can include data from discrete hall effect sensors, analog hall effect sensors, digital encoders, or resolvers. Necessary bandwidth for the position feedback varies with the maximum electrical frequency (maximum mechanical speed times the number of motor pole pairs). It is desirable that the feedback hardware slew rates are greater than the slew rate of the motor position at full speed, and that change in position is discernible over the noise background at all operating speeds. In general, resolvers yield the best results for the Atlas control platform, with the most resolution. Position feedback information can be processed through digital low-pass filters with user-settable gain. Advanced calibration algorithms can also be employed to adjust for position feedback non-idealities.

Speed limits (forward and backward), speed slew rates (acceleration), and speed-versus torque profiles are all settable per user requirements.

Limits and Protections

When configured as a motor controller, the Atlas firmware has several operating parameter limits and fault thresholds.

Current: The current limit is a limitation on the current demand that comes from the speed regulator. The current regulator will never try to drive a current higher than the current limit. If the actual current exceeds the current limit, then the current regulator will try to reduce the current. Above the current limit, a current fault threshold exists. If the actual current exceeds the current fault threshold, then a fault will be flagged, and the switching state machine will stop (transistors stop switching).

Speed: The speed limit is a limitation on the speed demand that comes from the user or external controller. The speed regulator will never try to drive a speed higher than the speed limit. If the actual speed exceeds the speed limit, then the speed regulator will try to reduce the motor speed. Above the speed limit, an overspeed fault threshold exists. If the actual speed exceeds the overspeed fault threshold, then a fault will be flagged, and the switching state machine will stop (transistors stop switching).

Voltage: Motor controllers typically do not regulate output or input voltages, therefore there is no voltage limit when operating the Atlas board as a motor controller. An input voltage fault threshold exists such that if the input voltage ever exceeds the threshold, a fault will be flagged, and the switching state machine will stop (transistors stop switching).

All limits and fault thresholds discussed above are settable per user requirements.

Other faults: The motor controller maintains several fail safe features to detect abnormal digital controls behavior such as loss communication with the host, or a logic lockup within either the DSP or FPGA. All of the fault scenarios listed below will generate a unique fault ID and halt the motor operation.

1) Loss of communication – If the controller does not receive a communication packet within 2x period of the normal communication period, a communication fault is declared.
2) DSP Watchdog timer – If the DSP does not receive an interrupt from the FPGA within a 2x period of the normal interrupt period, a DSP watchdog fault is declared.
3) FPGA Watchdog timer – If the FPGA's control register is not written to by the DSP within a 2x period of the normal PWM period, a FPGA watchdog fault is declared.
4) DSP Internal Watchdog – If the software on the DSP freezes, a watchdog timer integrated into the DSP silicon will trigger another fault.

Heat Dissipation

The Atlas control board dissipates a maximum of 4.5W, variable with logic load.

Field Weakening

If the motor BEMF magnitude plus voltage across the load impedance exceeds the DC link voltage, the motor can no longer be driven at unity power factor. If desired, field weakening can be used to drive the motor to higher speeds than would otherwise be achievable, at the cost of having to drive non-torque-producing current. The amount of speed gain per Amp of D-axis current (non-torque-producing) varies with the inductance of the stator's d-axis versus the field strength of the rotor. The speed threshold (RPM) at which field weakening starts can be set, and the amount of d-axis current driven per RPM over the threshold can be set (Amps/RPM). Care should be taken when setting these parameters so that the rotor does not get demagnetized.

Interface

Command Interface

Commands are passed through one of several available communication ports (RS232, RS485, or SPI). Modbus RTU is the default communication protocol. Custom protocols defined by the customer are easily implemented as requested.

Operational Command	Description	R/W	Units
CLRFLT	Clears faults	W	None
GET FLT	Returns present fault code	R	Unsigned integer
RUNSTOP	Sets the state of the motor drive	W	0 (stop) or 1 (run)
STATUS	Returns the status of the drive	R	Unsigned integer bitfield
SETSPEED	Sets speed command	W	RPM
GETSPEED	Get actual shaft speed	R	RPM
SETACC	Set acceleration rate	W	RPM/SEC
MAXTORQUE	Sets maximum torque limit	W	Nm
GETTORQUE	Get present torque	R	Nm
VDCBUS	Get VDC bus voltage	R	DC volts

Configuration Command	Description	R/W	Units
SENSOROFFSET	Shaft sensor offset	W	Degrees (0-360)
POLEPAIR	Sets the motor's number of magnetic pole pairs	W	Typically (8-20), integer
FBKRESOL	Specifies the shaft position feedback resolution	W	Integer 2^n (4096, 8192, etc)
IKP	Current loop proportional gain	W	Integer x 1000
IKI	Current loop integral gain	W	Integer x 1000
VKP	Velocity loop proportional gain	W	Integer x 1000
VKI	Velocity loop integral gain	W	Integer x 1000
KT	Sets motor torque constant	W	Nm/A, integer x 100
MAXSPEED	Maximum permissible speed	W	RPM, integer
MAXTEMP	Maximum permissible temperature	W	Celsius, integer

Feedback Interface(s)

Absolute mechanical shaft position is required. This can be provided by either a resolver or an absolute encoder. 3-phase current and DC link voltage measurements through an ADC are also necessary. Standard digital communication interfaces are supported (SPI, I2C, SSI, etc). Resolution of the feedback sensor is specified by customer and programmed at the factory.

Power Interface

Power is provided to the Atlas control board over select pins on the 200-pin SO-DIMM edge connector. The three voltages provided should meet the requirements below:

Voltage	Min voltage	Nom voltage	Max voltage	Min current
3.3 V	3.14	3.3	3.46	1.014 A
1.2 V	1.14	1.2	1.26	0.785 A
1.8V	1.71	1.8	1.89	0.050 A

Test and Data Interface

A 100 element fault history queue is always maintained with the motor controller. The faults are stored FILO (first in, last out) so that the most recent fault is at the top of the queue. The individual fault values are retrieved by specifying the fault index of the desired fault in time. Index #0 is the most recent; #1 is the next most recent, and so forth.

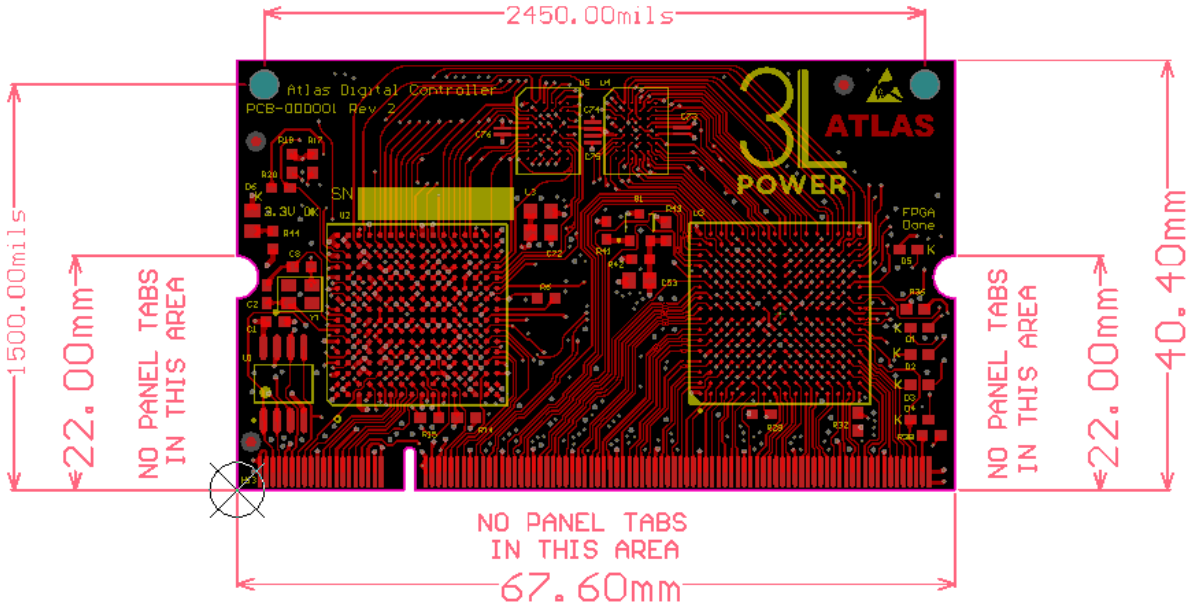
Fault Queue	Description	R/W	Units
FQINDEX	Specify the fault index	W	Integer (0 – 99)
FQNUMBER	Fault number	R	Integer
FQDATE	Fault date	R	Integer (MMDD)
FQTIME	Fault time	R	Integer (HHMM)
FQSEC	Fault second	R	Integer (SS)
FQINT	Fault interrupt counter	R	Integer (0 – 0xffff)

A 1000 record data collection history buffer of 12 elements each is always maintained by the motor controller. The controller updates the data buffer every PWM interrupt period with the user specified set of internal control variables. The data collection is halted upon a system fault, or by user request. The data history mechanism is useful for post fault analysis, or for general data observation.

Data History	Description	R/W	Units
DCSELECT	Selects which data set shall be monitored	W	Integer
DCSTRIDE	Sets the stride (collect every n^{th} interrupt)	W	Integer
DCTRIGGER	Selects the condition that will halt the collection.	W	Integer
DCSETSTATE	Command to halt the data collection.	W	Integer (0=halt,1= run)
DCGETSTATE	Returns the state of the data collection	R	Integer (0=halted,1=running)
DCINDEX	Specifies which record to present.	R	Integer (0 to 999)
DCVALUE0	Data element #0 of the selected record	R	Integer x 1000
DCVALUE1	Data element #1 of the selected record	R	Integer x 1000
DCVALUE2	Data element #2 of the selected record	R	Integer x 1000
DCVALUE3	Data element #3 of the selected record	R	Integer x 1000
DCVALUE4	Data element #4 of the selected record	R	Integer x 1000
DCVALUE5	Data element #5 of the selected record	R	Integer x 1000
DCVALUE6	Data element #6 of the selected record	R	Integer x 1000
DCVALUE7	Data element #7 of the selected record	R	Integer x 1000
DCVALUE8	Data element #8 of the selected record	R	Integer x 1000
DCVALUE9	Data element #9 of the selected record	R	Integer x 1000
DCVALUE10	Data element #10 of the selected record	R	Integer x 1000
DCVALUE11	Data element #11 of the selected record	R	Integer x 1000

Mechanical Interface

The Atlas board fits into a 200-pin SODIMM 1.8V header per JEDEC Standard MO-224E. TE Connectivity header 1827341-4 is an example of such a header. Board dimensions are shown in the diagram below. Additional 100-mil diameter mounting holes are positioned as shown below.



Environmental

Operating Environmental

Operating environmental temperature range:	-40°C to 85°C (industrial)
Operating vibration limit:	6G at 5 Hz to 20 kHz
Operating shock limit:	250G
Operating pressure:	3 psi to 10,000 psi

Non-operating Environmental

Storage temperature range:	-40°C to 150°C (industrial)
Non-operating vibration limit:	6G at 5 Hz to 20 kHz
Non-operating shock limit:	250G
Non-operating pressure:	3 psi to 10,000 psi

Pinout

The 200-pin Atlas Control Board has the following pinout:

SODIMM PIN#	TYPE	PIN	DESCRIPTION	CUSTOMER USAGE
1	GND		GND	--
2	PWR		1.8V (0.050A Max)	--
3	GND		GND	--
4	PWR		1.8V (0.050A Max)	--
5	DSP	T4	DSP SPI Chip Select for Atlas Flash Memory	
6	DSP	T10	DSP Reset Line, Pulled High on Atlas	
7	DSP	L2	DSP SPI Data In Line	
8	PWR		1.2V (0.785A Max)	--
9	GND		GND	--
10	NC		No Connect	--
11	DSP	M1	DSP SPI Clock Line	
12	DSP	P10	DSP JTAG EMU0	--
13	DSP	L1	DSP SPI Data Out Line	
14	PWR		3.3V (1.014A Max)	--
15	DSP	E3	DSP General Purpose I/O GPIO3	
16	DSP	F3	DSP General Purpose I/O GPIO6	
17	DSP	F1	DSP General Purpose I/O GPIO4	
18	DSP	G3	DSP General Purpose I/O GPIO9	
19	GND		GND	--
20	DSP	H3	DSP General Purpose I/O GPIO12	
21	DSP	F2	DSP General Purpose I/O GPIO5	
22	NC		No Connect	--
23	DSP	G1	DSP General Purpose I/O GPIO7	
24	DSP	T5	DSP SCI B Receive Line or GPIO23	
25	GND		GND	
26	DSP	R4	DSP SCI B Transmit Line or GPIO22	
27	DSP	G2	DSP General Purpose I/O GPIO8	
28	DSP	P7	DSP I2C SCL Line or GPIO33	
29	DSP	H1	DSP General Purpose I/O GPIO10	
30	DSP	R7	DSP I2C SDA Line GPIO32	
31	DSP	H2	DSP General Purpose I/O GPIO11	
32	DSP	R8	DSP JTAG TRST	--
33	PWR		1.2V (0.785A Max)	--
34	NC		No Connect	--

35	GND		GND	--
36	NC		No Connect	--
37	PWR		1.2V (0.785A Max)	--
38	DSP	T11	DSP JTAG TCK	--
39	GND		GND	--
40	DSP	R10	DSP JTAG EMU1	--
41	PWR		3.3V (1.014A Max)	--
42	DSP	P9	DSP JTAG TMS	--
43	GND		GND	--
44	DSP	T8	DSP JTAG TDI	--
45	PWR		3.3V (1.014A Max)	--
46	PWR		3.3V (1.014A Max)	--
47	NC		No Connect	--
48	DSP	P8	DSP JTAG TDO	--
49	NC		No Connect	--
50	FPGA	F8	FPGA General Purpose I/O	
51	DSP	P5	DSP CAN RX Line	
52	FPGA	F9	FPGA General Purpose I/O	
53	DSP	R4	DSP CAN TX Line	
54	FPGA	F13	FPGA General Purpose I/O	
55	GND		GND	--
56	FPGA	D14	FPGA General Purpose I/O	
57	DSP:	R6	DSP General Purpose I/O GPIO25	
58	FPGA	F11	FPGA General Purpose I/O	
59	FPGA	T10	FPGA General Purpose I/O	
60	FPGA	D13	FPGA General Purpose I/O	
61	FPGA	C4	FPGA General Purpose I/O	
62	FPGA	J11	FPGA General Purpose I/O	
63	FPGA	B15	FPGA General Purpose I/O	
64	FPGA	E13	FPGA General Purpose I/O	
65	GND		GND	--
66	NC		No Connect	--
67	FPGA	A15	True LVDS Pair - or General I/O	
68	FPGA	T9	FPGA General Purpose I/O	
69	FPGA	N6	FPGA General Purpose I/O	
70	FPGA	P10	FPGA General Purpose I/O	
71	FPGA	A14	True LVDS Pair + or General I/O	
72	FPGA	N9	FPGA General Purpose I/O	
73	FPGA	B13	FPGA General Purpose I/O	
74	FPGA	R10	FPGA General Purpose I/O	
75	GND		GND	--
76	PWR		1.2V (0.785A Max)	--
77	FPGA	A13	FPGA General Purpose I/O	
78	FPGA	R9	FPGA General Purpose I/O	

79	FPGA	B11	FPGA General Purpose I/O	
80	FPGA	N8	FPGA General Purpose I/O	
81	FPGA	A11	FPGA General Purpose I/O	
82	FPGA	R8	FPGA General Purpose I/O	
83	FPGA	B10	FPGA General Purpose I/O	
84	FPGA	T8	FPGA General Purpose I/O	
85	FPGA	A10	FPGA General Purpose I/O	
86	FPGA	P8	FPGA General Purpose I/O	
87	GND		GND	--
88	FPGA	C13	FPGA General Purpose I/O	
89	FPGA	B9	FPGA General Purpose I/O	
90	FPGA	F12	FPGA General Purpose I/O	
91	FPGA	A9	FPGA General Purpose I/O	
92	FPGA	E11	FPGA General Purpose I/O	
93	FPGA	A8	FPGA General Purpose I/O	
94	FPGA	D11	FPGA General Purpose I/O	
95	FPGA	B8	FPGA General Purpose I/O	
96	FPGA	C11	FPGA General Purpose I/O	
97	FPGA	A7	FPGA General Purpose I/O	
98	FPGA	D10	FPGA General Purpose I/O	
99	FPGA	B7	FPGA General Purpose I/O	
100	FPGA	C10	FPGA General Purpose I/O	
101	GND		GND	--
102	FPGA	D9	FPGA General Purpose I/O	
103	FPGA	A6	FPGA General Purpose I/O	
104	FPGA	C9	FPGA General Purpose I/O	
105	FPGA	B6	FPGA General Purpose I/O	
106	FPGA	C7	FPGA General Purpose I/O	
107	FPGA	A5	FPGA General Purpose I/O	
108	FPGA	D8	FPGA General Purpose I/O	
109	FPGA	A4	FPGA General Purpose I/O	
110	FPGA	D7	FPGA General Purpose I/O	
111	FPGA	B4	FPGA General Purpose I/O	
112	PWR		3.3V (1.014A Max)	--
113	GND		GND	--
114	FPGA	C6	FPGA General Purpose I/O	
115	FPGA	A3	FPGA General Purpose I/O	
116	FPGA	D6	FPGA General Purpose I/O	
117	FPGA	B3	FPGA General Purpose I/O	
118	FPGA	D5	FPGA General Purpose I/O	
119	FPGA	A2	FPGA General Purpose I/O	
120	FPGA	D3	FPGA General Purpose I/O	
121	FPGA	C3	FPGA General Purpose I/O	
122	FPGA	E8	FPGA General Purpose I/O	
123	FPGA	B2	FPGA General Purpose I/O	

124	FPGA	F7	FPGA General Purpose I/O	
125	FPGA	B1	FPGA General Purpose I/O	
126	FPGA	E6	FPGA General Purpose I/O	
127	GND		GND	--
128	FPGA	D4	FPGA General Purpose I/O	
129	FPGA	C2	FPGA General Purpose I/O	
130	FPGA	G6	FPGA General Purpose I/O	
131	FPGA	C1	FPGA General Purpose I/O	
132	FPGA	E5	FPGA General Purpose I/O	
133	FPGA	D2	FPGA General Purpose I/O	
134	FPGA	E4	FPGA General Purpose I/O	
135	FPGA	D1	FPGA General Purpose I/O	
136	FPGA	F5	FPGA General Purpose I/O	
137	FPGA	E1	FPGA General Purpose I/O	
138	FPGA	F4	FPGA General Purpose I/O	
139	FPGA	F1	FPGA General Purpose I/O	
140	FPGA	F6	FPGA General Purpose I/O	
141	GND		GND	--
142	FPGA	H3	FPGA General Purpose I/O	
143	FPGA	F2	FPGA General Purpose I/O	
144	FPGA	H4	FPGA General Purpose I/O	
145	FPGA	H1	FPGA General Purpose I/O	
146	FPGA	L5	FPGA General Purpose I/O	
147	FPGA	H2	FPGA General Purpose I/O	
148	FPGA	J4	FPGA General Purpose I/O	
149	FPGA	J1	FPGA General Purpose I/O	
150	FPGA	J5	FPGA General Purpose I/O	
151	FPGA	J2	FPGA General Purpose I/O	
152	FPGA	K3	FPGA General Purpose I/O	
153	FPGA	K1	FPGA General Purpose I/O	
154	FPGA	K4	FPGA General Purpose I/O	
155	FPGA	K2	FPGA General Purpose I/O	
156	FPGA	L3	FPGA General Purpose I/O	
157	GND		GND	--
158	FPGA	M4	FPGA General Purpose I/O	
159	FPGA	L1	FPGA General Purpose I/O	
160	FPGA	L4	FPGA General Purpose I/O	
161	FPGA	L2	FPGA General Purpose I/O	
162	FPGA	M5	FPGA General Purpose I/O	
163	FPGA	M1	FPGA General Purpose I/O	
164	FPGA	M6	FPGA General Purpose I/O	
165	FPGA	N1	FPGA General Purpose I/O	
166	FPGA	N3	FPGA General Purpose I/O	
167	FPGA	N2	FPGA General Purpose I/O	
168	FPGA	N4	FPGA General Purpose I/O	

169	FPGA	P1	FPGA General Purpose I/O	
170	PWR		3.3V (1.014A Max)	--
171	GND		GND	--
172	FPGA	P3	FPGA General Purpose I/O	
173	FPGA	P2	FPGA General Purpose I/O	
174	PWR		1.2V (0.785A Max)	--
175	FPGA	R1	FPGA General Purpose I/O	
176	FPGA	P4	FPGA General Purpose I/O	
177	FPGA	R2	FPGA General Purpose I/O	
178	FPGA	N6	FPGA General Purpose I/O	
179	FPGA	T2	FPGA General Purpose I/O	
180	FPGA	N5	FPGA General Purpose I/O	
181	FPGA	R3	FPGA General Purpose I/O	
182	PWR		3.3V (1.014A Max)	--
183	FPGA	T3	FPGA General Purpose I/O	
184	FPGA	P4	FPGA General Purpose I/O	
185	GND		GND	--
186	FPGA	P7	FPGA General Purpose I/O	
187	FPGA	R4	FPGA General Purpose I/O	
188	FPGA	N7	FPGA General Purpose I/O	
189	FPGA	T4	FPGA General Purpose I/O	
190	FPGA	G11	FPGA JTAG TMS	--
191	FPGA	T5	FPGA General Purpose I/O	
192	FPGA	T7	FPGA General Purpose I/O	
193	NC		No Connect	--
194	FPGA	R7	FPGA General Purpose I/O	
195	NC		No Connect	--
196	NC		No Connect	--
197	FPGA	H12	FPGA JTAG TDO	--
198	FPGA	H11	FPGA JTAG TCK	--
199	GND		GND	--
200	FPGA	G13	FPGA JTAG TDI	--